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10/648,608	08/25/2003	Peter W. Richards	P104-US	4234

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EXAMINER
KOVALICK, VINCENT E

ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,608	RICHARDS, PETER W.	
	Examiner	Art Unit	
	Vincent E. Kovalick	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-60* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-60* is/are allowed.

6)☒ Claim(s) *1-2, 4-7 and 14* is/are rejected.

7)☒ Claim(s) *3 and 8-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Applicant's reply, dated March 27, 2006, to USPTO Office Action dated December 28, 2005.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doherty (Pub. No. 2003/0227677) taken with Doherty et al. (6,201,521) in view of Pettitt et al. (USP 6,774,916).

Relative to claim 1, Doherty ('677) **teaches** a spatial light modulator (e.g. DMD) receives light form a color wheel and directs modulated light to a display (pg. 1, paras. 0009-0012); Doherty ('677) further **teaches** a method used in a display system that comprises an array of micromirrors, each micromirror being associated with one or more memory cell of a memory cell array, to produce images (pg., 1, paras. 0004-0007).

Doherty ('677) **does not teach** the method comprising: loading a pixel data matrix of the image; delivering the rows of the matrix in parallel into a data converter; transposing, by the data converter, the pixel data matrix into a bitplane matrix following a bitplane format wherein matrix elements in one row of the matrix represent one pixel of the image; and sending the bitplane

matrix into the memory cell array for actuating the micromirrors such that the image is produced by the micromirrors.

Doherty et al. ('521) **teaches** a divided reset for addressing spatial light modulator (col. 2, lines 31-62); Doherty (677) further **teaches** loading a pixel data matrix of the image; delivering the rows of the matrix in parallel into a data converter; transposing, by the data converter, the pixel data matrix into a bitplane matrix (col. 3, lines 54-65).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Doherty et al. ('677) the feature as taught by Doherty et al. ('521) in order to enable transitioning the pixel data matrix format to the bitplane matrix.

Doherty ('677) taken with Doherty ('521) **does not teach** a bitplane format wherein matrix elements in one row of the matrix represent one pixel of the image; and sending the bitplane matrix into the memory cell array for actuating the micromirrors such that the image is produced by the micromirrors.

Pettitt et al. **teaches** a display system using pulse width modulation (col. 3, lines 30-57); Pettitt et al. further **teaches** a biplane format wherein matrix elements in one row of the matrix represent one pixel of the image; and sending the bitplane matrix into the memory cell array for actuating the micromirrors such that the image is produced by the micromirrors (col. 4, lines 39-53).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Doherty et al. ('677) taken with Doherty et al. ('521) the feature as taught by Pettitt et al. in order to put the bitplane data into the memory cells which in turn will be reflected in the micromirrors.

Regarding claim 2, Pettitt further **teaches** the matrix elements in one column of the matrix represent one pixel of the image (col. 4, lines 39-53).

Relative to claim 6, Doherty ('521) further **teaches** the method step wherein the stem of sending the bitplane matrix into the memory call array further comprises: loading each row of the memory cells of the memory cell array tin at least a portion of a row of data element of the transposed pixel data matrix.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. as applied to claim 2 in item 3 hereinabove, and further in view of Lee et al. (Pub No. 2002/0080672).

Regarding claim 4, Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. **does not teach** the step of shifting the delayed data elements further comprising: loading the shifted data elements at each time-unit into a register of the data converter, the register having *n* bits, and sequentially shifting the loaded data elements such that the data element at bit *b* is shifted to bit *b*+1, and the data element at bit *n* is shifted to the first bit of the register.

Lee et al. **teaches** first-in first-out memory device and method of generating flag signal in the same (pg. 3m para. 0020).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. the feature as taught by Lee et al. in order to put the data elements in the proper time sequence for generating the data associated image.

5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. as applied to claim 1 in item 3 hereinabove, and further in view of Sandstedt et al. (Pub. No. 2002/0016629).

Relative to claim 5, Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. **does not teach** the method wherein the value of the data element of the matrix determines the voltage of a memory cell of the memory cell array, and the location of the matrix element in a column of the matrix determines the duration of the voltage in the memory cell such that the micromirror associated with said memory cell is turned on or off for the duration of said voltage.

Sandstedt et al. **teaches** a class of SLM devices that can be used in a digital micromirror device operating in reflection mode (pg. 1, paras. 0006-0011); Sandstedt et al. further **teaches** the method wherein the value of the data element of the matrix determines the voltage of a memory cell of the memory cell array, and the location of the matrix element in a column of the matrix determines the duration of the voltage in the memory cell such that the micromirror associated with said memory cell is turned on or off for the duration of said voltage (pg. 14, para. 0148).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. the feature as taught by Sandstedt et al. in order to control the time of reflection of the micromirror device based on the voltage content of the memory cell associated with a particular micromirror.

6. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. as applied to claim 1 in item 3 hereinabove, and further in view of Kuno et al. (Pub. No. 2003/0081132).

Regarding claim 7, Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. **does not teach** the method wherein the pixel data matrix is a square matrix having *m* x *m* data elements, wherein *m* (an integer greater than 1) equals 2(to the n power) and n is an integer greater than 1. **Kuno et al.** teaches an imaging apparatus and mobile terminal incorporating same (pg, 2, paras. 0018-9925); Kuno et al. further **teaches** the method wherein the pixel data matrix is a square matrix having *m* x *m* data elements, wherein *m* equals 2(to the n power) and n is an integer greater than 1 (pg. 2, para. 0018 and Abstract).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to provide to the device as taught by Doherty ('677) taken with Doherty ('521) in view of Pettitt et al. the feature as taught by Kuno et al. in order to provide an imaging apparatus that is easy to manufacture but has improved resolution in both the horizontal and vertical directions.

Allowable Subject Matter

7. Claims 3, 8-13 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 3, the major difference between the teachings of the prior art of record (Doherty (Pub. No. 2003/0227677) taken with Doherty et al. (6,201,521) in view of Pettitt et al. (USP 6,774,916)) and that of the instant invention is that said prior art of record **does not teach** the method step wherein the step of transposing the pixel data matrix into the bitplane matrix includes the steps of a) the data element of row *j* at the *k*(*th*) time-unit of the time-unit sequence

is shifted to row *j*-1 at the same time –unit; and the data element at row *l* of the *k*(*th*) time–unit is shifted to row *m* at the same time-unit, wherein *k* runs from1 to *m* + *n* time-units; and b) the date elements at the *n*(*th*) and *m*(*th*) time-unit are not shifted; and delaying the shifted data elements of the matrix according to the sequence of time-units such that a pixel data row *j* at tune-unit *p* is delayed *j* time-units relative to the data element of row *j*-1 at time-unit *p*.

Regarding claim 8, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a) transforming the pixel data matrix into a block matrix having 2x2 first order blocks, each first order block having 2x2 second order blocks, each second order block having 2x2 third order blocks, each *k*(*th*) order block having 2x2 (*k*+1)(*th*) order blocks, and the (*n*-1)(*th*) order block having 2x2 pixel data elements; b) transposing the pixel data matrix based on the first order blocks; c) transposing the pixel data matrix based on the *k*(*th*) order blocks after consecutive transposes of the pixel data matrix based on the first order block through the (*k*-1)(*th*) order blocks; and d) transposing the pixel data matrix based on the (*n*-1)(*th*) order blocks, each of which has 2x2 pixel data elements.

Regarding claim 9, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a) transforming the pixel data matrix into a block matrix having 2x2 first order blocks, each first order block having 2x2 second order blocks, each second order block having 2x2 third order blocks, each *k*(*th*) order block having 2x2 (*k*+1)(*th*) order blocks, and the (*n*-1)(*th*) order block having 2x2 pixel data elements; b) transposing the pixel data matrix based on the (*n*-1)(*th*) order blocks, each of which has 2x2 pixel data elements; c) transposing the pixel data matrix based on the *k*(*th*) order blocks after consecutive transposes of the pixel data matrix based on the (*n*-1)(*th)* order block through

the (*k*-1)(*th*) order blocks; and d) transposing the pixel data matrix based on the first order blocks,

Regarding claim 12, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** the method wherein the pixel data matrix having *m* x *n* date elements and wherein *m* is larger that *n;* and wherein the step of transposing further comprises: appending (*m*-*n*) rows to the matrix, wherein each appended row has *m* elements; and after transposing the matrix with the appended rows, truncating (*m*-*n*) data elements from each row of the transposed matrix.

Regarding claim 13, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** the method wherein the pixel data matrix having *m* x *n* date elements and wherein *m* is smaller that *n;* and wherein the step of transposing further comprises: appending (*m*-*n*) data elements to each row of the matrix; and after transposing the matrix with the appended rows, truncating (*m*-*n*) rows from the transposed matrix.

8. Claim 15-60 are allowed.

9. The following is an examiner's statement of reasons for allowance:

Relative to claim 15, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a display array of micromirrors comprising the method step of shifting the delayed data elements at each time-unit of the sequence of time-units according to a shifting rule, wherein the shifting rule states that: for a matrix having *m* columns and *n* rows a) the data element of row *j* at the *k*(*th*) time-unit of the time-unit sequence is shifted to row *j*-1 at the same time –unit; and the data element at row *l* of

the *k*(*th*) time–unit is shifted to row *m* at the same time-unit, wherein *k* runs from1 to *m* + *n* time-units; and b) the date elements at the *n*(*th*) and *m*(*th*) time-unit are not shifted; and delaying the shifted data elements of the matrix according to the sequence of time-units such that a pixel data row *j* at tune-unit *p* is delayed *j* time-units relative to the data element of row *j*-1 at time-unit *p*. Relative to claim 19, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** the method used in a display system comprising a array of micromirrors comprising the steps of transforming the pixel data matrix into a block matrix having 2x2 first order blocks, each first order block having 2x2 second order blocks, each second order block having 2x2 third order blocks, each *k*(*th*) order block having 2x2 (*k*+1)(*th*) order blocks, and the (*n*-1)(*th*) order block having 2x2 pixel data elements; transposing the pixel data matrix base on the (*n*-1)(*th*) order blocks, each of which has 2x2 pixel data elements; transposing the pixel data matrix based on the *k*(*th*) order blocks after consecutively transposes of the pixel data matrix base on the (*n*-1)(*th*) order block through the (*k*+1)(*th*) order blocks and transposing the pixel data matrix based on the first order blocks. Relative to claim 26, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** the method used in a display system comprising a array of micromirrors comprising a delay unit connected to the plurality of input lines, wherein the delay unit delays the received data such that: a) a data element at input line *j* at time-unit *k* is delayed one time-unit relative to the data element at input line *j* at time-unit *k*+1; and b) the data element is delayed one time-unit relative to the data element at input line *j*-1 at time-unit *k*; and a shifter connected to and receiving output data from

the delay unit wherein the shifter shifts the delayed data output from the first delay unit based on the sequence of time-units and according to a shifting rule, wherein the shifting rule states that: a) the data element of line *j* at the *k(th)* time-unit is shifted to line *j*-1 at the same time-unit; and the data element at line 1 at the *k(th)* time-unit is shifted to row m at the same time-unit, wherein *k* runs from 1 to *m*+*n* time-units; and b) the data elements at the *n(th)* and *m(th)* time-unit are not shifted.

Relative to claim 41, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** the method used in a display system comprising a array of micromirrors comprising: a multiplicity of sets of delay units, a) wherein a delay unit of the first set of delay units delays a data element one time-unit, and the delay units of the first set are connected to every two input lines, and b) wherein a delay unit of the *s(th)* set of delay unit delays a data 2(to the *s*-1 power) time-units, and the delay units of the *s(th)* set are connected to every 2(to the *s*-1 power) input lines; a plurality of sets of switches, a) wherein a switch of the first set of switches exchanges data elements between input lines 2*w*-1 and 2*w* with *s* running from 1 to *n*/2; and b) wherein a switch of the *s(th)* set of switches exchanges data elements between 2*w*-1 and (*n*/2)+*s*; and wherein each switch of the *s(th)* set of switches are located between the connected to two delay units of the *s(th)* set of delay units.

Regarding claim 43, the major difference between the teachings of the said prior art of record and that of the instant invention is that said prior art of record **does not teach** a display system comprising an array of micromirrors said system comprising: a first input line and a second input line that are associated with a sequence of time-units for receiving data elements; a first

delay unit that is connected to the second input line and delays the received data element one time-unit; a switch that is connected to the first input line and the first delay unit and receives data element from the output of the first delay unit, wherein the switch switches data elements between the first input line and the delayed data element output from the first delay unit; and a second delay unit that is connected to the first input line and delays the received data element one time-unit.

Response to Applicant's Remarks

10. Applicant's arguments filed March 27, 2006 have been fully considered but they are not persuasive.

Applicant argues that Doherty (USP 6,201,521) does not teach or suggest data conversion from pixel data to biplane data.

Doherty, (col. 3, lines 45-65) teaches display memory receives processed pixel data from processor system. It formats the data, on input or on output into "bit-plane" format and delivers the bit-planes to SLM one at a time. It would be obvious to a person of ordinary skill in the art at the time of the invention that to make the conversion of pixel matrix to bit-plane requires a converter (col. 3, lines 54-56); said converter would have to receive the pixel row data in parallel if said format was required to generate the said bit-plane.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,798,941	Smith et al.
U. S. Patent No.	5,442,458	Rabbani et al.
Pub. No.	2003/0197660	Marshall
Pub. No.	2003/0107539	Wood
Pub. No.	2002/0036611	Ishii

Final Rejection

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

To Respond

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E. Kovalick whose telephone number is 571-272-7669. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Vincent E. Kovalick
June 6, 2006

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